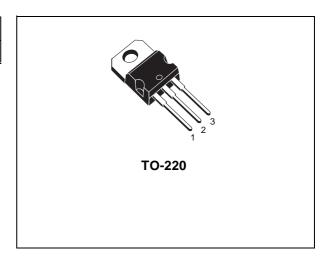


STP12NK30Z

N-CHANNEL 300V - 0.36Ω - 9A - TO-220 Zener-Protected SuperMESHTMPower MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D (1)	Pw (1)
STP12NK30Z	300 V	< 0.4 Ω	9 A	90 W

- TYPICAL $R_{DS}(on) = 0.36 \Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

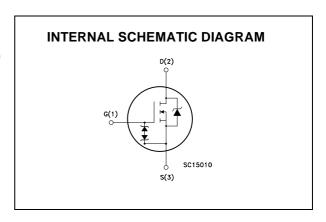


DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- LIGHTING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- HIGH CURRENT, HIGH SPEED SWITCHING



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP12NK30Z	P12NK30Z	TO-220	TUBE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	300	V
V_{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	300	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C Drain Current (continuous) at T _C = 100°C	9 5.6	A A
I _{DM} (1)	Drain Current (pulsed)	36	Α
P _{TOT}	Total Dissipation at T _C = 25°C	90	W
	Derating Factor	0.72	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000	V/ns
dv/dt (2)	Peak Diode Recovery voltage slope	4.5	V/ns
T _{stg}	Storage Temperature		
Tj	Max. Operating Junction Temperature		°C

THERMAL DATA

	Rthj-case	Thermal Resistance Junction-case Max	1.38	°C/W
Ī	Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
	T_I	Maximum Lead Temperature For Soldering Purpose	300	°C

Note: 1. Pulse width limited by safe operating area

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	9	А
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	155	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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^{2.} ISD< 9A, di/dt<300A/µs, VDD<V(BR)DSS, TJ<TJMAX

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	300			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu A$	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 4.5 A$		0.36	0.4	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 10 V, I _D = 4.5 A		5.4		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		670 125 28		pF pF pF
Coss eq. (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 440 V		70		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3.6		Ω

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise time Turn-off Delay Time Fall Time	V_{DD} = 150 V, I_D = 4.5 A R _G = 4.7 Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		16 20 36 10		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 240V, I_D = 9 A,$ $V_{GS} = 10V$		25 5.5 13.4	35	nC nC nC

SOURCE DRAIN DIODE

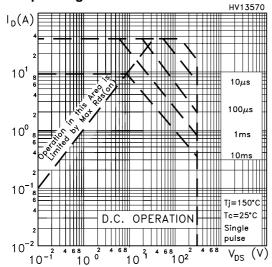
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				9 36	A A
V _{SD} (1)	Forward On Voltage	$I_{SD} = 9 A, V_{GS} = 0$			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 9$ A, di/dt = 100A/ μ s $V_{DD} = 40$ V, $T_j = 150$ °C (see test circuit, Figure 5)		165 0.9 11.2		ns µC A

Note: 1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

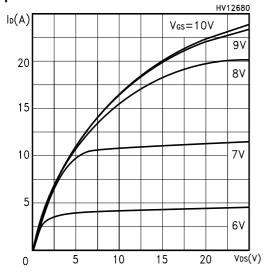
A7/.

Pulse width limited by safe operating area.
 C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

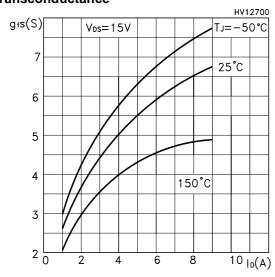
Safe Operating Area For TO-220



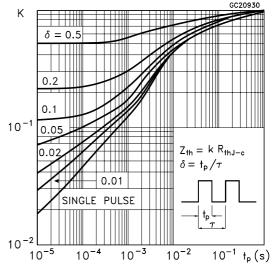
Output Characteristics



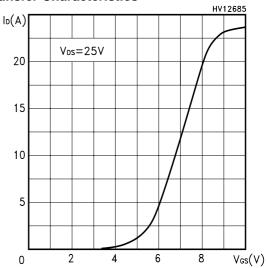
Transconductance



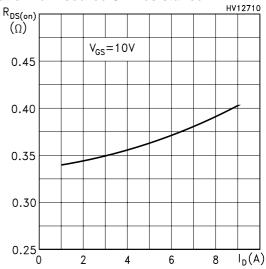
Thermal Impedance For TO-220



Transfer Characteristics

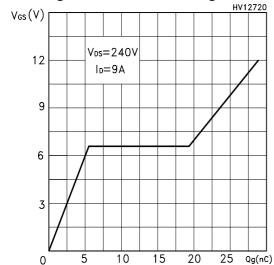


Static Drain-source On Resistance

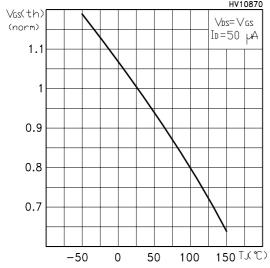


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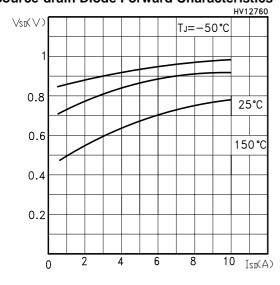
Gate Charge vs Gate-source Voltage



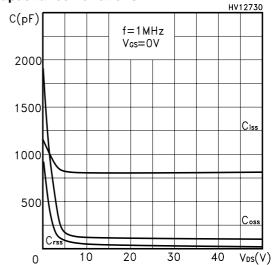
Normalized Gate Thereshold Voltage vs Temp.



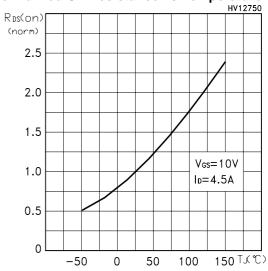
Source-drain Diode Forward Characteristics



Capacitance Variations



Normalized On Resistance vs Temperature



Normalized BVDSS vs Temperature

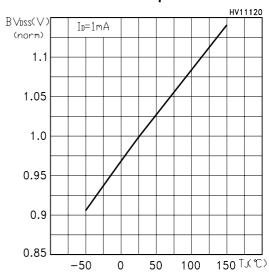


Fig. 1: Unclamped Inductive Load Test Circuit

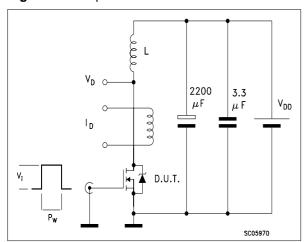


Fig. 3: Switching Times Test Circuit For Resistive Load

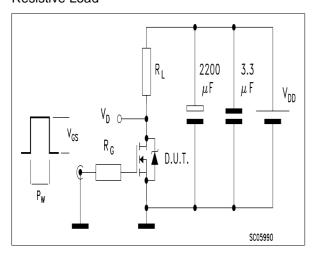


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

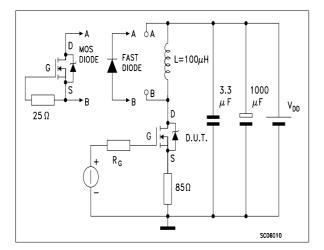


Fig. 2: Unclamped Inductive Waveform

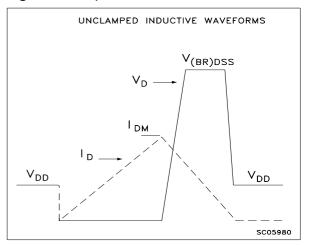
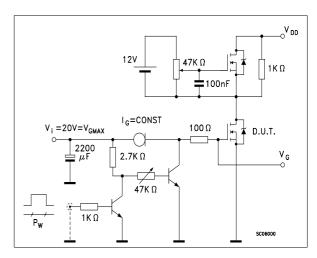


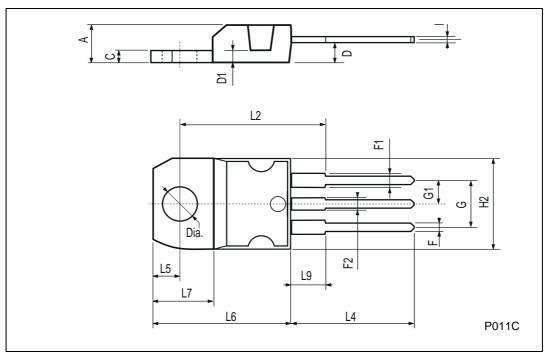
Fig. 4: Gate Charge test Circuit



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TO-220 MECHANICAL DATA

DIM.		mm			inch			
DIN.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
А	4.40		4.60	0.173		0.181		
С	1.23		1.32	0.048		0.051		
D	2.40		2.72	0.094		0.107		
D1		1.27			0.050			
E	0.49		0.70	0.019		0.027		
F	0.61		0.88	0.024		0.034		
F1	1.14		1.70	0.044		0.067		
F2	1.14		1.70	0.044		0.067		
G	4.95		5.15	0.194		0.203		
G1	2.4		2.7	0.094		0.106		
H2	10.0		10.40	0.393		0.409		
L2		16.4			0.645			
L4	13.0		14.0	0.511		0.551		
L5	2.65		2.95	0.104		0.116		
L6	15.25		15.75	0.600		0.620		
L7	6.2		6.6	0.244		0.260		
L9	3.5		3.93	0.137		0.154		
DIA.	3.75		3.85	0.147		0.151		



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